REMARKS/ARGUMENTS

The Office Action mailed August 15, 2003, has been received and reviewed. Claims 1, 3, 4, and 18 through 26 are currently pending in the application. Claims 1, 3, 4, and 18 through 26 stand rejected. Applicants have amended claims 1, 3, 4, 23 and 25, and respectfully request reconsideration of the application as amended herein.

Specification

Applicants note that various amendments have been made to the specification herein. Such Amendments are made in association with the revised drawing figures. No new matter has been added.

Drawings

Applicants submit herewith revised FIG. 4 (which has been revised to now identify it as FIG. 4A) and new FIG. 4B. Specifically, FIG. 4B is being submitted as a new drawing to address the Examiner's objection to the drawings under 37 CFR 1.83(a). No new matter has been added. Approval of the proposed revisions is respectfully requested.

Objection to the Drawings under 37 CFR 1.83(a)

The Examiner objects to the drawings as not showing every feature of the invention specified in the claims. Applicants respectfully disagree with the Examiner's objection and submit that all of the limitations of the claimed invention are shown in the drawings. Applicants note that 37 CFR 1.83(a) does not require that all of the features of a given claim be shown in a single drawing. Nevertheless, Applicants have provided new FIG. 4B which serves to bring multiple limitations of the various claims into a single drawing figure for sake of clarity and conciseness.

With respect to claims 1, 21 and 23, Applicants submit that every claimed feature is shown in the drawings. More particularly, Applicants direct the attention of the Examiner to FIGS. 2, 4A, 4B, and 7 through 9. Applicants note that the specific example set forth by the

Examiner of "at least one alignment feature electrically isolated from the plurality of conductors" is shown in FIGS. 4A and 4B (see, e.g., alignment features 450 and 450′).

Applicants, therefore, respectfully request reconsideration of the drawings and approval thereof.

35 U.S.C. § 102 Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,728,601 to Sato

Claims 3, 4 and 24 through 26 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Sato, U.S. Patent No. 5,728,601. Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claims 3 and 24 through 26

Independent claim 3, as amended herein, is directed to a method of forming an integrated circuit package. The method comprises: forming a leadframe having a plurality of conductors and at least one alignment feature; coupling at least some of the plurality of conductors to a semiconductor die; and encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material; and *electrically isolating the at least one alignment feature from the plurality of conductors*.

The Examiner cites Sato as disclosing a method of forming an integrated circuit package comprising: providing a plurality of conductors (24) and at least one alignment feature (23b); coupling at least some of the plurality of conductors to a semiconductor die (25); encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material (21). Applicants

submit, however, that Sato fails to teach *electrically isolating the at least one alignment feature from the plurality of conductors*.

Rather, referring to FIG. 5, Sato shows various bond pads electrically coupled to portions of the lead frame which are integral with the cutouts (23b) (which the Examiner cites as being alignment features). More specifically, Sato states that "some of the bonding pads 26 may be connected to the lead frame parts 23a and 23e for the ground connection." (Col. 6, lines 9-10). It is, therefore, clear that Sato fails to teach electrically isolating the at least one alignment feature from the plurality of conductors. As such, Sato fails to anticipate claim 3 of the presently claimed invention.

Applicants further submit that claims 24 through 26 are also allowable over Sato as being dependent from an allowable base claim as well as for the additional patentable subject matter introduced thereby.

With respect to claim 25, Applicants submit that Sato fails to teach disposing a heat spreader adjacent to, and in contact with, an external surface of the insulating material and, forming at least one other alignment feature in the heat spreader. While the Examiner states that the support leg (22) of Sato is a heat spreader which is coupled to "the external surface of the insulating material by fastening together and linking the heat spreader 22, *at least indirectly*, to the external surface of the insulating material," (Office Action, pages 5 and 6, emphasis added), Applicants note that there is no express or inherent teaching of Sato's support leg (22) being in contact with an external surface of the insulating material (21).

Applicants, therefore, respectfully request reconsideration and allowance of claims 3 and 24 through 26.

Claim 4

Independent claim 4, as amended herein, is directed to a method of forming and testing an integrated circuit package. The method comprises: forming a leadframe having a plurality of conductors and at least one alignment feature; electrically coupling at least some of the plurality of conductors to a semiconductor die; encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature

with an insulating material; *electrically isolating the at least one alignment feature from the plurality of conductors subsequent*; coupling the at least one alignment feature encompassed by the insulating material with a portion of a testing device; and testing the integrated circuit package through at least some of the electrically coupled conductors.

The Examiner cites Sato as disclosing a method of forming and testing an integrated circuit package, the method comprising: providing a plurality of conductors and at least one alignment features; electrically coupling at least some of the plurality of conductors to a semiconductor die; encompassing the semiconductor die a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material; coupling the at least one alignment feature encompassed by the insulating material with a portion of a testing device (the examiner points to the "conductor pattern provided on the substrate that may be a printed circuit board"); and testing the integrated circuit package through at least some of the electrically coupled conductors.

The Examiner states that it is inherent that the integrated circuit package is tested through at least some of the electrically coupled conductors when they are coupled to the circuit board and an attempt is made to operate the integrated circuit.

Applicants note that Sato fails to teach electrically isolating the at least one alignment feature from the plurality of conductors. Rather, as discussed above, teaches that the portions of the leadframe in which the cutouts (23b) are formed and coupled with the semiconductor die as a means of grounding the integrated circuit package. Thus, clearly, the conductors are in electrical communication by way of such grounding through the semiconductor die. As such, Sato fails to anticipate claim 4 of the presently claimed invention. Applicants, therefore, respectfully request reconsideration and allowance of claim 4.

Anticipation Rejection Based on U.S. Patent No. 6,420,195 to King

Claims 3, 4 and 24 stand rejected under 35 U.S.C. § 102(e) as being anticipated by King, U.S. Patent No. 6,420,195. Applicants respectfully traverse this rejection, as hereinafter set forth.

Claims 3 and 24

Independent claim 3, as amended herein, is directed to a method of forming an integrated circuit package. The method comprises: forming a leadframe having a plurality of conductors and at least one alignment feature; coupling at least some of the plurality of conductors to a semiconductor die; and encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material; and electrically isolating the at least one alignment feature from the plurality of conductors.

The Examiner cites King as disclosing a method of forming an integrated circuit package comprising: providing a plurality of conductors (44) and at least one alignment feature (50); coupling at least some of the plurality of conductors to a semiconductor die (42); and encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with and insulating material (46).

Applicants note, however, that King fails to teach *forming a lead frame* having a plurality of conductors and *at least one alignment feature*. Rather, the alignment features of the King device are formed as features in the surface of the integrated circuit package's molding compound. None of the embodiments disclosed by King appear to incorporate an alignment feature in a *leadframe*.

Applicants, therefore, respectfully submit that claim 3 is not anticipated by King. Applicants further submit that claim 24 is likewise allowable over King. With respect to claim 24, Applicants note that since King does not teach forming a lead frame having at least one alignment feature, that King can not be considered to form an alignment cut-out in the leadframe.

Applicants, therefore, respectfully request reconsideration and allowance of claims 3 and 24.

Claim 4

Independent claim 4, as amended herein, is directed to a method of forming and testing an integrated circuit package. The method comprises: *forming a leadframe having a plurality of conductors and at least one alignment feature*; electrically coupling at least some of the plurality of conductors to a semiconductor die; encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material; electrically isolating the at least one alignment feature from the plurality of conductors; coupling the at least one alignment feature encompassed by the insulating material with a portion of a testing device; and testing the integrated circuit package through at least some of the electrically coupled conductors.

The Examiner cites King as disclosing a method of forming and testing an integrated circuit package comprising: providing a plurality of conductors and at least one alignment features; electrically coupling at least some of the plurality of conductors to a semiconductor die; encompassing the semiconductor die a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material; coupling the at least one alignment feature encompassed by the insulating material with a portion of a testing device; and testing the integrated circuit package through at least some of the electrically coupled conductors.

However, King fails to teach forming a lead frame having a plurality of conductors and at least one alignment feature. As discussed above, the alignment features of the King device are formed as features in the surface of the integrated circuit package's molding compound. None of the embodiments disclosed by King appear to incorporate an alignment feature in a leadframe.

Applicants, therefore, submit that claim 24 is not anticipated by King and respectfully request reconsideration and allowance thereof.

Anticipation Rejection Based on U.S. Patent No. 4,689,875 to Solstad

Claims 1, 18 through 21 and 23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Solstad, U.S. Patent No. 4,689,875. Applicants respectfully traverse this rejection, as hereinafter set forth.

Claims 1 and 18 through 21

Independent claim 1, as amended herein, is directed to a method of forming an integrated circuit package. The method comprises: forming a lead frame having a plurality of conductors and at least one alignment feature; coupling at least some of the plurality of conductors to a semiconductor die; encapsulating the semiconductor die and a portion of the lead frame with an insulating material; *electrically isolating the at least one alignment feature from the plurality of conductors subsequent the encapsulating the semiconductor die and a portion of the lead frame with an insulating material;* and removing the at least one alignment feature subsequent the electrically isolating the at least one alignment feature from the plurality of conductors.

The Examiner cites Solstad as disclosing a method of forming an integrated circuit package comprising: forming a lead frame (10) having a plurality of conductors (16A, 16B) and at least one alignment feature (12A) electrically isolated from the plurality of conductors; coupling at least some of the plurality of conductors to a semiconductor die (20); encapsulating the semiconductor die and a portion of the lead frame with an insulating material (26, 32); and removing the at least one alignment feature subsequent the encapsulating the semiconductor die and a portion of the lead frame.

Solstad teaches the formation of an integrated circuit package using carrier tape wherein the carrier tape includes a metal layer (10A) bonded to a plastic insulating substrate (10B). A chip bonding area (13) is defined between sprocket openings (12A and 12B). A plurality of leads (16) of the metal layer are bonded to an integrated circuit chip (20). The leads are cut and bent to a desired position and an epoxy coating (32) is formed over the chip and leads. The integrated circuit package is then tested while still adhered to the carrier tape. If a package fails a test it is removed from the carrier tape. The carrier tape, along with the remaining integrated circuit packages, is wound on a reel for storage or transportation. (See, col. 4, line 21- col. 5, line 49).

Thus, it is clear that the process of Solstad does not electrically isolate the plurality of conductors from the sprocket opening *subsequent* the encapsulation of the chip with epoxy. Rather, in direct contrast with claim 1 of the presently claimed invention, the plurality of leads appear to become isolated from the remaining metal layer prior to any encapsulation process. As such, Applicants submit that claim 1 is not anticipated by Solstad.

Applicants further submit that claims 18 through 21 are allowable over Solstad as being dependent from an allowable base claim as well as for the additional patentable subject matter introduced thereby.

With respect to claim 21, Applicants submit that Solstad fails to teach perforating a separation line in a lead frame.

Applicants, therefore, respectfully request reconsideration and allowance of claims 1, and 18 through 21.

Claim 23

Independent claim 23, as amended herein, is directed to a method of forming and testing an integrated circuit package. The method comprises: forming a lead frame having a plurality of conductors and at least one alignment feature; coupling at least some of the plurality of conductors to a semiconductor die; encapsulating the semiconductor die and a portion of the lead frame with an insulating material; *electrically isolating the at least one alignment feature from the plurality of conductors subsequent the encapsulating the semiconductor die and a portion of the lead frame with an insulating material*; coupling the at least one alignment feature with a portion of a testing device; testing the integrated circuit package through at least some of the electrically coupled conductors; decoupling the at least one alignment feature from the portion of the testing device; and removing the at least one alignment feature subsequent the decoupling the at least one alignment feature from the portion of the testing device.

As set forth above, Applicants submit that Solstad fails to teach electrically isolating the at least one alignment feature from the plurality of conductors *subsequent* the encapsulating the semiconductor die and a apportion of the lead frame with an insulating material. Rather, in direct contrast with claim 23 of the presently claimed invention, Solstad teaches that the plurality

of leads appear to become isolated from the remaining metal layer prior to any encapsulation process. As such, Applicants submit that claim 23 is not anticipated by Solstad.

Applicants, therefore, respectfully request reconsideration and allowance of claim 23.

Anticipation Rejection Based on U.S. Patent No. 4,961,107 to Geist

Claims 1 and 18 through 22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Geist, U.S. Patent No. 4,961,107. Applicants respectfully traverse this rejection, as hereinafter set forth.

Independent claim 1, as amended herein, is directed to a method of forming an integrated circuit package. The method comprises: forming a lead frame having a plurality of conductors and at least one alignment feature; coupling at least some of the plurality of conductors to a semiconductor die; encapsulating the semiconductor die and a portion of the lead frame with an insulating material; *electrically isolating the at least one alignment feature from the plurality of conductors subsequent the encapsulating the semiconductor die and a portion of the lead frame with an insulating material; and removing the at least one alignment feature subsequent the electrically isolating the at least one alignment feature from the plurality of conductors.*

The Examiner cites Geist as disclosing a method of forming an integrated circuit package comprising: forming a lead frame (10) having a plurality of conductors (20) and at least one alignment feature (12) electrically isolated from the plurality of conductors; coupling at least some of the plurality of conductors to a semiconductor die (26); encapsulating the semiconductor die and a portion of the lead frame with an insulating material (36); and removing the at least one alignment feature subsequent the encapsulating the semiconductor die an a portion of the lead frame.

Applicants submit, however, that Geist fails to teach *electrically isolating the at least one alignment feature from the plurality of conductors subsequent the encapsulating the semiconductor die and a portion of the lead frame with an insulating material; and removing the at least one alignment feature subsequent the electrically isolating the at least one alignment feature from the plurality of conductors.* Rather, Geist discloses a new leadframe configuration

to accommodate improved heat transfer. In FIG. 5, Geist shows that the two portions of the leadframe (i.e., the die bonding portion 14 and the heat spreader portion 16) are interconnected as part of the leadframe strip through appropriate support members. After bonding of lead fingers to the semiconductor die, and also after encapsulation, the side rails (22) are removed from the leadframe. Geist notes that "[m]eans and methods for forming such leadframes, and attaching die 26 and wires 34 and providing encapsulation 36 *are well known in the art*." (Col. 3, lines 51-54, emphasis added). Thus, Geist does not teach any new subject matter with regard to the process of forming an integrated circuit package in terms of attaching a leadframe to a semiconductor die, encapsulating the die and leadframe, and excising extraneous tying components (e.g., side rails) from the lead frame.

It is clear that Geist's rails remain in electrical communication with the leads until the rails are excised and removed. As such, the electrical isolation and the removal of rails occurs *simultaneously*. In other words, the removal of the rails does not occur *subsequently* to the electrical isolation of the rails from the plurality of lead fingers. As such, claim 1 is clearly not anticipated by Geist.

Applicants further submit that claims 18 through 22 are also allowable over Geist at least by virtue of their dependency from an allowable base claim.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,728,601 to Sato in view of U.S. Patent 6,420,195 to King

Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Sato (U.S. Patent No. 5,728,601) as applied to claim 4 supra, and further in combination with King (U.S. Patent No. 6,420,195). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must

> be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claim4 is improper because The references relied upon fail to teach or suggest all of the limitations of claim 4 of the presently claimed invention.

Claim 4, as amended herein, is directed to a method of forming and testing an integrated circuit package. The method comprises: forming a leadframe having a plurality of conductors and at least one alignment feature; electrically coupling at least some of the plurality of conductors to a semiconductor die; encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material; *electrically isolating the at least one alignment feature from the plurality of conductors subsequent*; coupling the at least one alignment feature encompassed by the insulating material with a portion of a testing device; and testing the integrated circuit package through at least some of the electrically coupled conductors.

The Examiner notes that "Sato does not appear to literally teach coupling the at least one alignment feature encompassed by the insulating material with a portion of a testing device; and testing the integrated circuit package through at least some of the electrically coupled conductors." (Office Action, page 7). However, the Examiner cites King as teaching such subject matter. The Examiner then states that it would have been obvious to combine the process of King with the process of Sato because it would enable package testing and improve manufacturing quality.

Applicants note that, as discussed above, neither Sato nor King teach or suggest electrically isolating an alignment feature formed in the leadframe from a plurality of conductors also formed in the leadframe.

Rather, Sato teaches that the portions of the leadframe in which the cutouts (23b) are formed are electrically coupled with the semiconductor die as a means of grounding the

integrated circuit package. Thus, clearly, the conductors are in electrical communication with the cutouts by way of such grounding.

Additionally, the alignment features of the King device are formed as features in the surface of the integrated circuit package's molding compound. None of the embodiments disclosed by King appear to incorporate an alignment feature formed in a leadframe.

As such, Applicants submit that claim 4 is allowable over Sato and King and respectfully request reconsideration and allowance thereof.

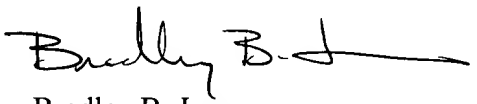
ENTRY OF AMENDMENTS

The amendments to claims 1, 3, 4, 23 and 25 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1, 3, 4, and 18 through 26 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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